WHAT IS CLAIMED IS:

1. A data storage device having parallel memory planes, comprising:

a first array plane of resistive cross point memory cells;

a second array plane of resistive cross point memory cells;

a plurality of conductive word lines shared between the first and second planes of memory cells;

a plurality of bit lines, each bit line coupling one memory cell from the first plane to another memory cell in the second plane;

a plurality of unidirectional element wherein one unidirectional element couples one memory cell from the first plane to a selected word line and a selected bit line in a first conductive direction and another unidirectional element couples another memory cell from the second plane to the selected word line and selected bit line in a second conductive direction.

2. The data storage device of claim 1 wherein a unidirectional conductive path forms from a memory cell in the first plane to a memory cell in the second plane sharing the same word line.

3. The data storage device of claim 1, further comprising multiple read circuits each coupled to one or more groups of memory cells by a respective bit line and operable to sense current flow through a memory cell of the associated groups.

4. The data storage device of claim 3, wherein each read circuit comprises a sense amplifier.

5. The data storage device of claim 4, wherein the sense amplifier is a current mode sense amplifier.

6. The data storage device of claim 4, wherein unselected word lines in a selected group of word lines are connected to a voltage that is approximately equal to an applied voltage on the inputs of the sense amplifier.

7. The data storage device of claim 6, wherein the unselected word lines are bias to the same potential as the selected bit line.

8. The data storage device of claim 1, comprising an equipotential generator coupled to the word lines and operable to set voltage levels in the resistive cross point memory cell array to substantially prevent or divert selected parasitic currents from interfering with the sense current from adjacent memory cells not being read.

9. The process of claim 8, wherein the equipotential generator is operable to set an input node of the common unidirectional element of each group of memory cells to block feedback from unselected word lines representing a common array voltage.

10. The data storage device of claim 1, wherein each memory cell comprises a magnetic tunnel junction element.

11. The data storage device of claim 1, wherein each memory cell comprises a phase change element.

12. A process of making a data storage device, comprising:

forming a plurality of word lines;

forming a plurality of bit lines; and

forming a first array plane of resistive cross point memory cells, each memory cell coupled to a respective bit line and coupled to a respective word line;

forming a second array plane of resistive cross point memory cells, each memory cell coupled to a respective bit line and a respective word line, wherein one cell from the first array plane and one cell from the second array plane share a common bit line and word line;

biasing the array so that a current flows from the common word line through the cell from the first array to the common bit line;

blocking the current from flowing through the cell from the second array during the biasing of the array.

13. The process of claim 12 comprising during the read process forming a unidirectional conductive path from the word line to the bit line through the memory cell.

14. The process of claim 12, further comprising forming multiple read circuits each coupled to one or more memory cells by a respective bit line and operable to sense current flow through any memory cell coupled thereto.

15. The process of claim 14, wherein each read circuit comprises a sense amplifier.

16. The process of claim 15, wherein the sense amplifier is operable to compare current flowing through a selected memory cell with a reference current to produce resistance state of the memory cell.

17. The process of claim 13, further comprising forming an equipotential generator coupled to the word lines and operable to set voltage levels in the resistive

cross point memory cell array to substantially prevent or divert selected parasitic currents from interfering with the sense current from memory cells.

18. The process of claim 17, wherein the equipotential generator is operable to set an input node of the common isolation diode of each group of memory cells from feedback from unselected word lines representing a common array voltage.